AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A data transmission system ~~for carrying out data transmission/reception~~, comprising:

a primary board;

secondary boards; and

a data transmission path carrying out data transmission/reception between ~~a~~ the primary board and the secondary boards ~~by using a data transmission path~~, ~~which~~ the data transmission path employs a same signal line as an address bus and a data bus mutually, ~~comprising:~~

wherein ~~informing a start address required for data access~~ when the data access is executed from the primary board to the secondary boards, informing a start address required for data access,~~;~~ and

~~generating~~ wherein an address used in the data access in the secondary boards is generated based on the start address, a predetermined trigger signal and a cycle signal indicating switching of data, the cycle signal is combined with the trigger signal.

2. (canceled).

3. (original): The data transmission system according to claim 1, wherein, when the address is generated based on the trigger signal, the address is generated sequentially by incrementing the start address in response to a timing of the trigger signal.

4. (canceled).

5. (currently amended): A data transmission system comprising:

a primary board;

secondary boards; and

a data transmission path for carrying out data transmission/reception between ~~a~~ the primary board and the secondary boards ~~by using a data transmission path~~, where the data transmission path ~~which~~ employs a same signal line as an address bus and a data bus mutually, ~~comprising:~~

wherein:

~~informing a memory start address of the secondary boards required for data access~~ when the data access is executed from the primary board to the secondary boards, informing a memory start address of the secondary boards required for data access,;

judging in the secondary boards whether or not the memory start address is directed to own station, and then executing the data transmission via the data transmission path by accessing a memory in own station based on the memory start address when the memory start address is directed to own station,; and

~~generating~~ an address is generated, to which the data transmission is subsequently executed, in the secondary boards by incrementing the memory start address after the data transmission based on the memory start address is ended, and then executing the data transmission via the data transmission path by accessing the memory of own station based on the generated address, and

wherein a cycle signal indicating switching of data is used in combination with a trigger signal.

6. (currently amended): A data transmission system comprising:

a primary board;

secondary boards; and

a data transmission path for carrying out data read between ~~a~~ the primary board and the secondary boards ~~by using a data transmission path~~, wherein ~~which~~ the data transmission path employs a same signal line as an address bus and a data bus mutually, ~~comprising the steps of:~~

wherein the data transmission system executes the following step in carrying out data transmission:

informs~~ing~~ a trigger signal combined with a cycle signal indicating a timing of data access, and a start address required for data read via the data transmission path~~,~~;

switches~~ing~~ the data transmission path to which the start address is informed as a data bus~~,~~;

accesses~~ing~~ a memory based on the start address and sending out a read result onto the data transmission path~~,~~; and

incrementsing the start address at a timing of the trigger signal, and then sending out a read result onto the data transmission path by accessing the memory based on the incremented address.

7. (canceled).

8. (currently amended): A data transmission system comprising:

a primary board;

secondary boards; and

a data transmission path for carrying out data write between a the primary board and the secondary boards by using a data transmission path, where the data transmission path which employs a same signal line as an address bus and a data bus mutually, comprising the steps of: wherein the carrying out of the data transmission/reception is executed by:

informing a trigger signal combined with a cycle signal indicating a timing of data access and a start address required for data write via the data transmission path,;

switching the data transmission path to which the start address is informed as a data bus, and then sending out a predetermined data to be written to a memory;

accessing the memory based on the start address, and then writing the predetermined data into the memory,; and

incrementing the start address at a timing of the trigger signal, and then writing sequentially the predetermined data, that are sent out via the data transmission path, into the memory by accessing the memory based on the incremented address.

9. (canceled).

10. (new): A method for carrying out data write between a primary board and secondary boards by using a data transmission path, which employs a same signal line as an address bus and a data bus mutually, comprising:

informing a trigger signal combined with a cycle signal indicating a timing of data access and a start address required for data write via the data transmission path;

switching the data transmission path to which the start address is informed as a data bus, and then sending out a predetermined data to be written to a memory;

accessing the memory based on the start address, and then writing the predetermined data into the memory; and

incrementing the start address at a timing of the trigger signal, and then writing sequentially the predetermined data, that are sent out via the data transmission path, into the memory by accessing the memory based on the incremented address.